IN THE CLAIMS

1-11. (Previously Canceled)

12. (Currently Amended) An array of planar T-RAM cells comprising:

a plurality of T-RAM cells, said plurality of T-RAM cells being arranged in an array and fabricated over a substrate, each of said plurality of T-RAM cells including a buried vertical thyristor and a horizontally stacked pseudo-TFT transfer gate, said horizontally stacked pseudo-TFT transfer gate including a source/drain and body formed in a polysilicon layer, said thyristor being buried underneath said horizontally stacked pseudo-TFT transfer gate, wherein said horizontally stacked pseudo-TFT transfer gate covers the entire top surface of said thyristor, and further wherein the top surface of said horizontally stacked pseudo-TFT transfer gate forms a co-planar top surface of each said horizontally stacked pseudo-TFT transfer gate of each said T-RAM cell.

13. (Previously Canceled)

14. (Original) The array according to Claim 12, wherein each of the plurality of T-RAM cells has a size of less than or equal to $8F^2$.

15. (Previously Amended) The array according to Claim 12, wherein said substrate is a semiconductor SOI or bulk wafer.

16. (Previously Amended) The array according to Claim 13, wherein a base of said thyristor is surrounded by a surrounded gate.

17. (Previously Amended) The array according to Claim 12, wherein said planar top surface of each T-RAM cell provides for fabrication of wordlines, said wordlines being fabricated over said planar top surface of said T-RAM cells, said wordlines for interconnecting said T-RAM cells.

18-31. (Previously Canceled)